

ABSTRACT OF THE DISCLOSURE

A memory controller provides programmable flexibility, via one or more
5 configuration registers, for the configuration of the memory. The memory may be
optimized for a given application by programming the configuration registers. For
example, in one embodiment, the portion of the address of a memory transaction used to
select a storage location for access in response to the memory transaction may be
programmable. In an implementation designed for DRAM, a first portion may be
10 programmably selected to form the row address and a second portion may be
programmable selected to form the column address. Additional embodiments may
further include programmable selection of the portion of the address used to select a bank.
Still further, interleave modes among memory sections assigned to different chip selects
and among two or more channels to memory may be programmable, in some
15 implementations. Furthermore, the portion of the address used to select between
interleaved memory sections or interleaved channels may be programmable. One
particular implementation may include all of the above programmable features, which
may provide a high degree of flexibility in optimizing the memory system.